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Donald L. Bartels
Coudert Brothers LLP
3458 ELLICOTT CENTER DRIVER SUITE 101
ELLICOTT CITY, MD 94306-2121

EXAMINER
NATNAEL, PAULOS M

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2614	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/693,351	DING ET AL.
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>20 September 2004</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8-12,14 and 16-22* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6,8-12,14,16,17,19 and 20* is/are rejected.

7)☒ Claim(s) *18,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2.   Claim **14** is rejected under 35 U.S.C. 102(e) as being anticipated by Tinker et al.,

U.S. Patent # 6,456,329.

Considering claim **14,**

(a) separating a video image frame into its component fields where a first one of

said component fields is associated with a display time preceding that of a second one

of said component fields each of said component fields including a plurality of pixel

lines, is met by Fig.1.

(b) determining which of said component fields is said first component field, is inherent,

because in order to process the field, the system must know which one is which.

(c) selecting one of said first component field and said second component field of said

video image frame for processing to a filtered video frame, is met by Fig.4;

(d) setting a first pixel line of said filtered video frame to a first pixel line of said

component field selected in step (c), is met by (line a) fig.5;

(e) setting said second pixel line of said filtered video frame to said first pixel line

of said component field selected in step (c) if said selected component field is said

second component field, is met by (line b) fig.5;

(f) generating a pixel line having pixel values equal to an average of corresponding

pixels in each adjacent pair of pixel lines of said selected component field, is met by

(right shifted on a per-pixel basis(For divide by 2), fig. 5.

 (g) inserting said generated pixel line between said corresponding adjacent pair

of pixel lines of said filtered video frame except said first pixel line and said second pixel

line if said selected component field is said second component field, is met by final of

processed pixels, Fig.5. (see also col. 6, lines 12-42)

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1,2, and 4-6, 8-13,16, 17, 19, 20** are rejected under 35 U.S.C. 103(a) as being

unpatentable over **Adams** et al., U.S. Pat. No. 6,380,978.

Considering claim **1**, Adams et al disclose the following claimed subject matter, note;

a) the claimed navigation unit operative to isolate an input video signal, is met by video

data buffer 42, (fig.3).

b) the claimed a decoder operative to separate said input video signal into a plurality of

frames, each frame containing a series of fields, is met by the Deinterlacing stage 1,

fig.4; (see also fig.5 and col. 9, lines 24+)

d) a processing unit responsive to said indication of said processing type entry for

providing a filtered video frame from a corresponding one of said plurality of frames for

display on a progressive display device, is met by video output processor 60, fig.4;

        Except for;

c) the claimed detection unit <u>having means for generating a look-up table prior to</u>

<u>processing said plurality of frames for display, said look-up table including a processing</u>

type associated with a corresponding one of said plurality of frames, said detection unit

further having means for providing an indication of said processing type entry

corresponding to said each frame from said look-up table; and,

Regarding c), Adams does not specifically disclose generating a look-up table.

However, Adams discloses a deInterlacer stage 1 (70) and a deInterlacer stage 2 (80).

DeInterlacer stage 1 (70) performs progressive frame sequence **detection** and field

difference processing, while the deInterlacer stage 2 (80) performs vertical frequency

detection, signal reversal **detection** and diagonal feature **detection**. The SDRAM

controller controls data going in and out of the SDRAMs. Furthermore, Adams discloses

detecting current, last, and next fields and processing either field difference processing

or frequency detection (fig.7). Further, Adams discloses "Combining fields into frames

as shown in Fig.5 requires identification of the type of motion picture used in the original

source." (col. 9, lines 37-40) It is also obvious from Figs.4-6 that Adams uses algorithms

or software/computer programs stored in the SDRAM, controlled by the SDRAM

controller, and the programs are generated as needed to control the various detection

processes in de-interlacing process in the image enhancement engine. Therefore, it

would have been obvious to those with ordinary skill in the art at the time the invention

was made to modify the reference of Adams by providing the well known in the art look-

up table or some sort of an algorithm to generating the various **detections** the de-

interlacer stages perform before processing the frames (or video signal) so that the

system would have an organized and efficient process of detecting the type of

processing that is needed to be performed to each frame or field.

Considering claim **2,** wherein said input video signal is isolated from a digital versatile

disk (DVD) inserted into said navigation unit, is met by DVD Media Transport 22, fig. 3,

which outputs the input video to video data buffer 42.

Considering claim **4,** the device of Claim 1, wherein third processing type entry induces

execution of a third processing algorithm in said processing unit upon said indication

thereof said third processing algorithm producing said filtered video frame from the field

data of said each frame and a predetermined number of preceding frames;

      See rejection of claim 1(c).

Claim **5** (Currently amended): The device of Claim 4, wherein said predetermined

number of preceding frames is three, is met by Fig. 5;

Claim **6** (Currently amended): The device of Claim 1, wherein a second processing type

entry induces execution of a second processing algorithm in said processing unit upon

said indication thereof said second processing algorithm producing said filtered video

frame by concatenating said fields of said each frame, is met by the output of FIFOs

136, 138 140 to field assembly 150, which in turn outputs a frame 152. (see also

rejection of claim 1(c) and fig.5)

Considering claim **8,** a digital video display system, comprising:

a) a navigation module operative to isolate an input video signal present in a digital medium is met by video data buffer 42, fig.3;

b) a decoder operative to separate said input video signal into a plurality of video frames, is met by the De-interlacing stage 1, fig.4; (see also fig.5 and col. 9, lines 24-35+)

d) a processing module responsive to said indication of said processing type entry for providing a filtered video frame for display on a progressive display device, said filtered video frame processed in accordance with one of said processing type entry and said user selection of processing type, is met by video output processor 60, fig.4, which performs horizontal scaling, color space conversion, dithering, and gamma, contract and brightness processing in order to ready the RGB video output signals for display on a display device.

Except for;

c) a detection module having means for generating a look-up table prior to processing said plurality of frames for display, said look-up table including a processing type associated with a corresponding one of said plurality of frames, said detection unit further having means for providing an indication of said processing type entry corresponding to said each frame from said look-up table, said detection module further including means for user selection of processing type for said each video frame, said user selection overriding said processing type entry thereof;

Regarding c), see rejection of claim 1(c).

Considering claim **9**, wherein said processing unit further comprises a first processing module operative to provide a digital video frame that is a concatenation of fields of an input data frame, and a second processing module operative to provide a digital video frame containing field segments having values based on adjacent field segments is met by the output of FIFOs 136, 138 140 to field assembly 150, which in turn outputs a frame 152. (see also fig.5)

Considering claim **10**, The system of Claim 8, wherein said detection module is further includes means for determining the type of processing to be performed on said video frame based on field data of a predetermined number of prior video frames and said video frame, is met by deinterlacers 70 and 80, fig.4. (see also fig.5)

Considering claim **11**, the claimed "wherein the predetermined number of prior video frames is three", is met by Fig. 5;

Considering claim **12**, Adams et al disclose the following claimed subject matter, note;

a) obtaining current video information from an input video signal, is met by video data buffer 42, fig.3;

b) separating said input video signal into plurality of video frames, is met by fig. 5, which

shows the input signals is separated into fields and then into frames.

c) a detecting if each said video frame matches an entry in predetermined table, for

specifying a processing type, is met by Deinterlacers 70 and 80, Fig.4, which performs

frame sequence detection or frequency detection, determining *whether field difference*

processing should be performed using the FIFO/Addressing and separating circuits 90

as storage or memory. (see Fig.4, which clearly illustrates also that de-interlacers 70

and 80 perform progressive frame sequence detection and vertical frequency detection,

respectively).

Except for;

d) generating a look-up table having a plurality of processing type entries prior to

processing said plurality of video frames. each of said processing type entries

respectively storing an indication of a processing algorithm for processing field data of a

corresponding one of said plurality of video frames;

e) retrieving one of said plurality of processing type entries corresponding to one of said

plurality of video frame frames prior to the display thereof;

f) processing said one of said video frames in accordance with said processing

algorithm indicated by said corresponding processing type entry.

Regarding d), see rejection of claim 1(c).

Regarding e) and f), see rejection of claim 4.

Claim **16** (Currently amended): The device of Claim 1, wherein said detection unit is

further includes means for user selection of processing type for said each frame said

user selection overriding said processing type entry thereof;

      Regarding claim 16, see rejection of claim 1(c).

Regarding new added claim **17**, see rejection of claim 1(c).

Regarding new added claim **19**, see also rejection of claim 1(c).

Regarding new added claim **20**, see rejection of claim 6.

Response to Arguments

Applicant's Argument

a) It is submitted that equating the data structure with memory hardware by which it may

be stored appears to be attempt to fit the disclosure of Adams via the application of

hindsight to the invention of the subject Patent application.

b) The invention of the subject patent application provides an independent processing

choice on a frame by frame basis, whereas the frames processed by the invention of

Adams are ultimately processed identically.

c) All of the references cited by the Examiner fail to show, or even suggest, "means for

generating a look-up table prior to processing [a] plurality of frames for display" ...

d) The invention ...requires the <u>identification of the fields so that applicable processing</u> <u>may be applied</u>. That is to say, for example, when the field is to be presented as the later of the two fields in a frame, the first pixel line of the field is inserted as the first two (2) pixel lines of the processed frame....this distinction is reflected in amended claim 14....As noted by the Examiner, Callahan treats both fields equally. Thus, Callahan actually <u>teaches away</u> from processing the individual fields by respectively performing different processing thereon.

Examiner Response

a) Applicant is right in that Adams does not specifically disclose generating a look-up table. However, as shown above in the rejection of claim 1, Adams discloses a delnterlacer stage 1 (70) and a delnterlacer stage 2 (80). Delnterlacer stage 1 (70) performs progressive frame sequence **detection** and field difference processing, while the delnterlacer stage 2 (80) performing vertical frequency **detection**, signal reversal **detection** and diagonal feature **detection.** The SDRAM controller controls data going in and out of the SDRAMs. Furthermore, Adams discloses detecting current, last, and next fields and processing either field difference processing or frequency detection (fig.7). Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the reference of Adams by providing a look-up table (which is notoriously well-known in the art) for generating the various **detections** the de-interlacer

stages perform, before processing the frames (or video signal) so that the system would

have an organized process of detecting the type of processing that needs to be

performed to each frame or field.

b) It's not clear what is meant by "ultimately processed identically". However, it is clear

from Adams' Fig.5 of Adams that the processing is done frame by frame. Argument

therefore is unpersuasive in this regard.

c) See rejection of claim 1(c) and part A above.

d)see rejection of claim 14.

Allowable Subject Matter

4.   Claims **18, 21-22** are objected to as being dependent upon a rejected base

claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims.

5.   The following is a statement of reasons for the indication of allowable subject

matter: the prior art fails to disclose a video signal processing method comprising,

wherein said third processing type entry is a null entry into said look-up table, said

indication thereof corresponding to no predetermined processing type associated with

said corresponding frame, as in claim 18; and, whereby a video frame processing step

includes, multiplying pixel values of each field line in each of the plurality of video

frames by a corresponding scaling value, and summing adjacent scaled field lines when the processing type entry indicates a second processing algorithm, as in claim **21**.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
December 31, 2004

PAULOS M. NATNAEL
PATENT EXAMINER